Amendments to the Claims

This listing of claims will replace all prior versions and listings of claims in the application:

Listing of claims:

1. - 11. (cancelled)

12. (currently amended) The apparatus for a signal-triggered digital circuit, said apparatus comprising:

a signal source for generating a digital signal;

an input receiver, said input receiver receiving said digital signal for said digital circuit and being responsive to triggering induced by said digital signal;

a conducting interface;

a conducting signal path, said conducting signal path being electrically connected to said conducting interface at a corner thereof, said conducting interface being electrically connected to said input receiver, said signal path carrying said digital signal thereover said conducting signal path having a length which is at least 1/6th of a transition electrical length of said digital signal carried thereover, said transition electrical length constituting a transient time of said digital signal multiplied by a propagation speed of said digital signal over said conducting signal path, and wherein said transient time of the said digital signal is selected from a group comprising a rise time thereof and a fall time thereof; and

wherein said conducting interface is substantially rectangular in planar view and said conducting signal path connected thereto as aforesaid has a longitudinal centerline axis which forms an angle in a range of 110 to 160 degrees with respect to a side of said conducting interface to which said conducting signal path is connected to thereby produce a reduced reflection of said digital signal at said connection between said conducting interface and said conducting signal path when compared to a connection wherein said angle has a value of 90 degrees.

13. - 14. (canceled)

15. (currently amended) The apparatus according to Claim [[14]] 12, wherein said conducting signal path has a length which is at least said transition electrical length of said digital signal carried thereover.

16. (currently amended) The apparatus according to Claim [[13]] 12, wherein said angle in a range of 110 to 160 degrees is an angle of 135 degrees.

17. (previously presented) The apparatus according to Claim 16, further comprising a circuit substrate, wherein said input receiver and said conducting interface are located on said circuit substrate.

18. (previously presented) The apparatus according to Claim 17, wherein said circuit substrate comprises a printed circuit board and wherein said conducting interface is a pad and said conducting signal path is a trace.

19. (previously presented) The apparatus according to Claim 18, wherein said pad is substantially square in planar view.

20. (previously presented) The apparatus according to Claim 18, wherein said trace has a width which is 1/5th of a width of said pad to which said trace is connected.

21. (previously presented)The apparatus according to Claim 18, wherein when said input receiver is mounted to said pad, said trace has a thickness which is in a range of 1/5th to 1/6th of a thickness of said pad to which said trace is connected.

22. (previously presented) The apparatus according to Claim 18, wherein when said input receiver is mounted to said pad, said pad has a width of 22 mils and a thickness in a range of 6 mils to 7 mils, and wherein said trace has a width of 4 mils and a thickness of 1.2 mils.

23. (previously presented) The apparatus according to Claim 18, wherein the apparatus is a memory system which further comprises a memory device, wherein said signal source is a

memory controller which generates digital signals in the form of control signals carried by said trace, and wherein said input receiver is located within said memory device.

24. (previously presented) The apparatus according to Claim 23, wherein said circuit substrate further comprises a slot and wherein said memory system further comprises a memory module on which said memory device is located, said memory module being a dual in-line memory module (DIMM) comprising an edge connector, said DIMM being connected to said memory controller by said edge connector connecting to said slot.

25. (currently amended) The circuit substrate for a signal-triggered digital circuit, said circuit substrate comprising:

a conducting interface, substantially rectangular in planar view, for electrical connection to an input receiver, said input receiver receiving a digital signal over said digital circuit and being responsive to triggering induced by said digital signal;

a conducting signal path having a width which is 1/5th of a width of said conducting interface, said conducting signal path being connected to said conducting interface, said signal path carrying said digital signal thereover, said conducting signal path having a thickness which is in a range of 1/5th to 1/6th of a thickness of the conducting interface to which said conducting signal path is connected; and

wherein said conducting signal path connected to said conducting interface has a longitudinal centerline axis which forms an angle in a range of 110 to 160 degrees with respect to a side of the conducting interface to which said conducting signal path is connected to thereby produce a reduced reflection of said digital signal at said connection between said conducting interface and said conducting signal path when compared to a connection wherein said angle has a value of 90 degrees.

26. (previously presented) The circuit substrate according to Claim 25, wherein said conducting interface is substantially square in planar view.

27. (canceled)

28. (previously presented) The circuit substrate according to Claim 25, wherein when said input receiver is mounted to said conducting interface, said conducting interface has a width of 22 mils and a thickness in a range of 6 mils to 7 mils, and wherein said conducting signal path has a width of 4 mils and a thickness of 1.2 mils.

29. (previously presented) The circuit substrate according to Claim 25, wherein said conducting signal path is connected to the conducting interface at a corner thereof.

30. (previously presented) The circuit substrate according to Claim 29, wherein said conducting signal path has a length which is at least 1/6th of a transition electrical length of said digital signal carried thereover, said transition electrical length constituting a transient time of said digital signal multiplied by a propagation speed of said digital signal over said conducting signal path, and wherein said transient time of said digital signal is selected from a group comprising a rise time thereof and a fall time thereof.

31. (previously presented) The circuit substrate according to Claim 30, wherein said conducting signal path has a length which is at least said transition electrical length of said digital signal carried thereover.

32. (previously presented) The circuit substrate according to Claim 29, wherein said angle in a range of 110 to 160 degrees is an angle of 135 degrees.

33. (previously presented) The circuit substrate according to Claim 32, wherein said circuit substrate comprises a printed circuit board, said conducting interface is a pad and said conducting signal path is a trace.

34. (previously presented) The circuit substrate according to Claim 33, said circuit substrate further comprising an input receiver and a signal source for generating said digital signal.

35. (previously presented) The circuit substrate according to claim 34, said circuit substrate further comprising a memory device, wherein said signal source is a memory controller which

generates digital signals in the form of control signals carried by said trace, and wherein said input receiver is located within said memory device.

36. (previously presented) The circuit substrate according to Claim 35, wherein said circuit substrate further comprises a slot and wherein said memory system further comprises a memory module on which said memory device is located, said memory module being a dual in-line memory module (DIMM) comprising an edge connector, said DIMM being connected to said memory controller by said edge connector connecting to said slot.

37. (previously presented) The apparatus for a signal-triggered digital circuit of a memory system device, said apparatus comprising:

a memory controller signal source for generating a digital control signal;

an input receiver located within said memory device, said input receiver receiving said digital signal for said digital circuit and being responsive to triggering induced by said digital signal;

a conducting interface;

a conducting signal path, said conducting signal path being electrically connected to said conducting interface at a corner thereof, said conducting interface being electrically connected to said input receiver, said signal path carrying said digital signal thereover, said conducting signal path having a length which is at least $1/6^{th}$ of a transition electrical length of said digital signal carried thereover, said transition electrical length constituting a transient time of said digital signal multiplied by a propagation speed of said digital signal over said conducting signal path, said transient time of the said digital signal being selected from a group comprising a rise time thereof and a fall time thereof; and

wherein said conducting interface is substantially rectangular in planar view and said conducting signal path connected thereto as aforesaid has a longitudinal centerline axis which forms an angle in a range of 110 to 160 degrees with respect to a side of said conducting interface to which said conducting signal path is connected to thereby produce a reduced reflection of said digital signal at said connection between said conducting interface and said conducting signal path when compared to a connection

wherein said angle has a value of 90 degrees.

38. – 39. (cancelled)

40. (previously presented) The apparatus according to Claim 37, wherein said conducting signal path has a length which is at least said transition electrical length of said digital signal carried thereover.

41. (previously presented) The apparatus according to Claim 37, wherein said angle in a range of 110 to 160 degrees is an angle of 135 degrees.

42. (previously presented)The apparatus according to Claim 41, further comprising a circuit substrate, wherein said conducting interface and said conducting signal path are located on said circuit substrate.

43. (previously presented) The apparatus according to Claim 42, wherein said circuit substrate comprises a printed circuit board and wherein said conducting interface is a pad and said conducting signal path is a trace.

44. (previously presented) The apparatus according to Claim 43, wherein said pad is substantially square in planar view.

45. (previously presented) The apparatus according to Claim 43, wherein said trace has a width which is 1/5th of a width of said pad to which said trace is connected.

46. (previously presented) The apparatus according to Claim 43, wherein when said input receiver is mounted to said pad, said trace has a thickness which is in a range of 1/5th to 1/6th of a thickness of said pad to which said trace is connected.

47. (previously presented) The apparatus according to Claim 43, wherein when said input receiver is mounted to said pad, said pad has a width of 22 mils and a thickness in a range of 6

mils to 7 mils, and wherein said trace has a width of 4 mils and a thickness of 1.2 mils.

48. (previously presented) The apparatus according to Claim 42, wherein said circuit substrate further comprises a slot and wherein said memory system further comprises a memory module on which said memory device is located, said memory module being a dual in-line memory module (DIMM) comprising an edge connector, said DIMM being connected to said memory controller by said edge connector connecting to said slot.

49. (previously presented) The circuit substrate for a signal-triggered memory device digital circuit, said circuit substrate comprising:

a conducting interface, substantially rectangular in planar view, for electrical connection to an input receiver of the memory device, said input receiver receiving a digital control signal over said digital circuit and being responsive to triggering induced by said digital control signal;

a conducting signal path having a width which is 1/5th of a width of said conducting interface, said conducting signal path being connected to said conducting interface, said signal path carrying said digital control signal thereover, said conducting signal path having a thickness which is in the range of $1/5^{th}$ to $1/6^{th}$ of a thickness of the conducting interface to which said conducting signal path is connected; and

wherein said conducting path connected to said conducting interface has a longitudinal centerline axis which forms an angle in a range of 110 to 160 degrees with respect to a side of the conducting interface to which said path is connected to thereby produce a reduced reflection of said digital control signal at said connection between said conducting interface and said conducting path when compared to a connection wherein said angle has a value of 90 degrees.

50. (previously presented)The circuit substrate according to Claim 49, wherein said conducting interface is substantially square in planar view.

51. (cancelled)

52. (previously presented) The circuit substrate according to Claim 49, wherein when said input receiver is mounted to said conducting interface, said conducting interface has a width of 22 mils and a thickness in a range of 6 mils to 7 mils, and wherein said conducting signal path has a width of 4 mils and a thickness of 1.2 mils.

53. (previously presented) The circuit substrate according to Claim 49, wherein said conducting signal path is connected to the conducting interface at a corner thereof.

54. (previously presented) The circuit substrate according to Claim 53, wherein said conducting signal path has a length which is at least 1/6th of a transition electrical length of said digital signal carried thereover, said transition electrical length constituting a transient time of said digital signal multiplied by a propagation speed of said digital signal over said conducting signal path, and wherein said transient time of said digital signal is selected from a group comprising a rise time thereof and à fall time thereof.

55. (previously presented)The circuit substrate according to Claim 54, wherein said conducting signal path has a length which is at least said transition electrical length of said digital signal carried thereover.

56. (previously presented) The circuit substrate according to Claim 53, wherein said angle in a range of 110 to 160 degrees is an angle of 135 degrees.

57. (previously presented) The circuit substrate according to Claim 56, wherein said circuit substrate comprises a printed circuit board, said conducting interface is a pad and said conducting signal path is a trace.

58. (previously presented) The circuit substrate according to Claim 57, said circuit substrate further comprising a signal source for generating said digital control signal.

59. (currently amended) The circuit substrate according to Claim 58, wherein said circuit substrate further comprises a slot and wherein said memory device further comprises a memory

module on which said memory device is located, said memory module being a dual in-line memory module (DIMM) comprising an edge connector, said DIMM being connected to said memory ~~controller~~ device by said edge connector connecting to said slot.